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Serial No. 10/077,778

IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~striketrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please ADD new claims 49 - 83 in accordance with the following:

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46. (CANCELLED)

47. (CANCELLED)

48. (CURRENTLY AMENDED) A memory device, comprising:

a nonvolatile memory connected to a first memory bus, and capable of storing data received thereby through said first memory bus;

a volatile memory connected to a second memory bus, and capable of being random-accessed through said second memory bus; and

a controller having a first internal terminal connected to said first memory bus, a second internal terminal connected to said second memory bus, and an external terminal connected to an external bus, said controller ~~for~~ transferring data between said nonvolatile memory and said volatile memory through said first and second internal terminals, wherein:

wherein, when the data transfer is not performed, said controller controls to access from an exterior to said volatile memory through said external terminal and said second internal terminal, in accordance with an instruction through said external bus, and said controller performs error detection and/or correction processing in said data transfer.

49. (NEW) The memory device according to claim 48, wherein said controller includes a register capable of storing a source address, a destination address, and a size of data to be transferred.

50. (NEW) The memory device according to claim 48, wherein said controller performs data transfer between said volatile memory and said nonvolatile memory in accordance with an external instruction without affecting said external bus.

51. (NEW) The memory device according to claim 50, wherein said controller notifies said external bus of an end of the data transfer by an interrupt.

52. (NEW) The memory device according to claim 48, wherein said controller temporarily stops the data transfer by a suspend command in a data transfer between said nonvolatile memory and said volatile memory, accesses said volatile memory in accordance with

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an external instruction, and then resumes the data transfer by a resume command.

53. (NEW) The memory device according to claim 48, wherein said nonvolatile memory, said volatile memory, and said controller are incorporated in a single package.

54. (NEW) The memory device according to claim 48, wherein said controller is capable of starting writing a plurality of data units in said volatile memory or said nonvolatile memory before said plurality of data units have been completely read out from said nonvolatile memory or said volatile memory in data transfer between said nonvolatile memory and said volatile memory.

55. (NEW) The memory device according to claim 54, wherein said controller starts writing a plurality of data units in said volatile memory before said plurality of data units have been completely read out from said nonvolatile memory in data transfer from said nonvolatile memory to said volatile memory.

56. (NEW) The memory device according to claim 54, wherein said controller starts writing a plurality of data units in said nonvolatile memory before said plurality of data units have been completely read out from said volatile memory in data transfer from said volatile memory to said nonvolatile memory.

57. (NEW) The memory device according to claim 54, wherein said controller reads out actual data and error detection and correction data from said nonvolatile memory, performs error detection and/or correction processing for said actual data on the basis of said error detection and correction data, and writes said actual data in said volatile memory, in data transfer from said nonvolatile memory to said volatile memory.

58. (NEW) The memory device according to claim 54, wherein said controller reads out actual data from said volatile memory, generates error detection and correction data on the basis of said actual data, and writes said actual data and said error detection and correction data in said nonvolatile memory, in data transfer from said volatile memory to said nonvolatile memory.

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59. (NEW) The memory device according to claim 54, wherein said controller further comprises an error detection and correction register storing error detection and correction information.

60. (NEW) The memory device according to claim 59, wherein said error detection and correction register stores an address of data from which an error has been detected.

61. (NEW) The memory device according to claim 54, wherein said controller further comprises a buffer buffering data and performing said data transfer through said buffer.

62. (NEW) The memory device according to claim 61, wherein said controller performs said data transfer in a time interval obtained by adding one transfer cycle to a time interval obtained by multiplying a transfer cycle by the number of transfer data.

63. (NEW) The memory device according to claim 48, wherein said controller reads out actual data, error detection and correction data from said nonvolatile memory, performs error detection for said actual data on the basis of said error detection and correction data, writes said actual data in said volatile memory, and performs error correction processing for said actual data on said volatile memory, in data transfer from said nonvolatile memory to said volatile memory.

64. (NEW) The memory device according to claim 48, wherein said controller includes a memory bus, connected to said nonvolatile and volatile memories, and an external bus, externally connected, said external bus having a single input/output voltage level and said memory bus and said external bus having different input/output voltage level ranges.

65. (NEW) The memo device according to claim 64, wherein said nonvolatile and volatile memories have different operable input/output voltage level ranges.

66. (NEW) The memory device according to claim 65, wherein said controller accesses said nonvolatile and volatile memories using an overlap range of the operable input/output voltage levels of said plurality of memories.

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67. (NEW) The memory device according to claim 66, wherein said controller comprises a power supply terminal inputting a power supply voltage at an input/output voltage level within said overlap range and controls input/output voltage levels of said nonvolatile and volatile memories on the basis of a voltage of said power supply terminal.

68. (NEW) The memory device according to claim 65, wherein said controller accesses said nonvolatile and volatile memories using different input/output voltage levels which do not overlap.

69. (NEW) The memory device according to claim 68, wherein said controller comprises two power supply terminals inputting power supply voltages at different input/output voltage levels which do not overlap and controls input/output voltage levels of said nonvolatile and volatile memories on the basis of voltages of said two power supply terminals.

70. (NEW) The memory device according to claim 68, wherein operable input/output voltage level ranges of said nonvolatile and volatile memories do not overlap.

71. (NEW) A memory device, comprising:
a nonvolatile memory including an actual data area storing a plurality of actual data units and a spare data area storing a plurality of spare data units;
a volatile memory including an actual data area storing a plurality of actual data units and a spare data area storing a plurality of spare data units; and
a controller for performing data transfer between said nonvolatile memory and said volatile memory.

72. (NEW) The memory device according to claim 71, wherein each of said spare data units includes one of control information and management information.

73. (NEW) The memory device according to claim 71, wherein said plurality of actual data units and said plurality of spare data units are in a one-to-one correspondence.

74. (NEW) The memory device according to claim 71, wherein said actual data area and said spare data area in said volatile memory are provided as continuous address areas.

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75. (NEW) The memory device according to claim 74, wherein said actual data area and said spare data area in said nonvolatile memory are provided as discontinuous address areas.

76. (NEW) The memory device according to claim 73, wherein said controller decomposes actual and spare data units which have been correspondingly read out from said actual data area and said spare data area in said nonvolatile memory, and writes the decomposed actual and spare data units respectively in said actual data area and said spare data area in said volatile memory, in data transfer from said nonvolatile memory to said volatile memory.

77. (NEW) The memory device according to claim 73, wherein said controller includes a first write controller linking actual and spare data units which have been correspondingly read out from said actual data area and said spare data area in said volatile memory, and writing the linked actual and spare data units respectively in said actual data area and said spare data area in said nonvolatile memory, in data transfer from said volatile memory to said nonvolatile memory.

78. (NEW) The memory device according to claim 73, wherein said controller includes a spare data register storing one or more spare data units, links an actual data unit in said actual data area in said volatile memory and a spare data unit in said spare data register, and writes the linked actual and spare data units, respectively in said actual data area and said spare data area, in said nonvolatile memory.

79. (NEW) The memory device according to claim 78, wherein said spare data register stores one spare data unit.

80. (NEW) The memory device according to claim 78, wherein said controller writes a plurality of spare data units in said nonvolatile memory using one spare data unit in said spare data register when said plurality of spare data units have the same contents.

81. (NEW) The memory device according to claim 77, wherein said controller further comprises a second write controller, including a spare data register storing one or more spare data units, said second write controller linking an actual data unit in said actual data area in said

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volatile memory and a spare data unit in said spare data register and writing the linked actual and spare data units respectively in said actual data area and said spare data area in said nonvolatile memory.

82. (NEW) The memory device according to claim 81, wherein said controller selects which of said first and second write controllers is used to write.

83. (NEW) The memory device according to claim 48 wherein:
said controller has an assign terminal for externally inputting an assign signal; and
when the assign signal is input to said assign terminal, said controller performs an assignment between said first internal terminal and said external terminal.